

CLAIMS:

1. A semiconductor structure comprising:
  - (a) a silicon substrate;
  - (b) a layer of aluminum directly overlying a first surface of said substrate;
  - (c) a polycrystalline nucleation layer of a nitride semiconductor directly overlying said aluminum layer;
  - (d) a buffer structure including one or more superlattices overlying said nucleation layer, each said superlattice including a plurality of nitride-based semiconductors of different compositions; and
  - (e) an operative structure of one or more gallium nitride-based semiconductors overlying said buffer structure.
2. A structure as claimed in claim 1 wherein said buffer structure includes a first superlattice, an intermediate layer of a nitride-based semiconductor overlying the first superlattice, and a second superlattice overlying the intermediate layer.
3. A structure as claimed in claim 2 wherein each of said first and second superlattices consists essentially of semiconductors according to the formula  $\text{Al}_r\text{Ga}_{(1-r)}\text{N}$  where  $0 \leq r \leq 1$ .
4. A structure as claimed in claim 3 wherein each of said first and second superlattices consists of only two semiconductors having different values of  $r$ .
5. A structure as claimed in claim 4 wherein the semiconductors included in said first superlattice are the same as the semiconductors included in said second superlattice.
6. A structure as claimed in claim 3 wherein said first superlattice directly overlies said nucleation layer.
7. A structure as claimed in claim 6 wherein said nucleation layer consists essentially of aluminum nitride.

8. A structure as claimed in claim 1 wherein said buffer structure includes a first superlattice directly overlying said nucleation layer.

9. A structure as claimed in claim 6 wherein said nucleation layer consists essentially of aluminum nitride.

10. A structure as claimed in claim 1 wherein said operative structure includes a first layer of nitride semiconductor; said structure further comprising at least one first metal layer overlying said first layer of nitride semiconductor and forming a Schottky contact therewith.

11. A structure as claimed in claim 10 wherein said first layer of nitride semiconductor includes a gallium-nitride-based semiconductor.

12. A structure as claimed in claim 10 wherein said first layer of nitride semiconductor includes GaN.

13. A structure as claimed in claim 10 further comprising at least one further metal layer overlying a second surface of said silicon substrate and forming an ohmic contact therewith.

14. A structure as claimed in claim 10 wherein said operative structure includes a further layer of nitride semiconductor disposed between said first layer of nitride semiconductor and said buffer structure; said further layer of nitride semiconductor having a higher doping concentration than that of said first layer of nitride semiconductor.

15. A structure as claimed in claim 14 wherein said further layer of nitride semiconductor includes a gallium nitride-based semiconductor.

16. A structure as claimed in claim 14 wherein said further layer of nitride semiconductor includes GaN.

17. A structure as claimed in claim 10 wherein said first layer of nitride semiconductor overlays an entire width of said buffer structure, and said first metal layer overlays an entire width of said first layer of nitride semiconductor.

18. A structure as claimed in claim 10 wherein said first layer of nitride semiconductor overlays a portion of said buffer structure, and said first metal layer overlays an entire width of said first layer of nitride semiconductor.

19. A semiconductor structure comprising:

- (a) a silicon substrate;
- (b) a polycrystalline nucleation layer of a nitride semiconductor overlying a surface of said substrate;
- (c) a buffer structure including a first superlattice directly overlying said nucleation layer, said first superlattice including a plurality of nitride-based semiconductors of different compositions; and
- (e) an operative structure of one or more gallium nitride-based semiconductors overlying said buffer structure.

20. A structure as claimed in claim 19 wherein said nucleation layer consists essentially of aluminum nitride and said first superlattice consists essentially of semiconductors according to the formula  $\text{Al}_r\text{Ga}_{(1-r)}\text{N}$  where  $0 \leq r \leq 1$ .

21. A structure as claimed in claim 19 wherein said buffer structure includes an intermediate layer of a nitride-based semiconductor overlying said first superlattice, and a second superlattice including a plurality of nitride-based semiconductors overlying the intermediate layer.

22. A structure as claimed in claim 21 wherein each of said first and second superlattices consists essentially of semiconductors according to the formula  $\text{Al}_r\text{Ga}_{(1-r)}\text{N}$  where  $0 \leq r \leq 1$ .

23. A structure as claimed in claim 22 wherein each of said first and second superlattices consists of only two semiconductors having different values of  $r$ .

24. A structure as claimed in claim 23 wherein the semiconductors included in said first superlattice are the

same as the semiconductors included in said second superlattice.

25. A structure as claimed in claim 19 wherein said operative structure includes a first layer of nitride semiconductor; said structure further comprising at least one first metal layer overlying said first layer of nitride semiconductor and forming a Schottky contact therewith.

26. A structure as claimed in claim 25 wherein said first layer of nitride semiconductor includes a gallium nitride-based semiconductor.

27. A structure as claimed in claim 25 wherein said first layer of nitride semiconductor includes GaN.

28. A structure as claimed in claim 25 further comprising at least one further metal layer overlying another surface of said silicon substrate and forming an ohmic contact therewith.

29. A structure as claimed in claim 25 wherein said operative structure includes a further layer of nitride semiconductor disposed between said first layer of nitride semiconductor and said buffer structure; said further layer of nitride semiconductor having a higher doping concentration than that of said first layer of nitride semiconductor.

30. A structure as claimed in claim 29 wherein said further layer of nitride semiconductor includes a gallium nitride-based semiconductor.

31. A structure as claimed in claim 29 wherein said further layer of nitride semiconductor includes GaN.

32. A structure as claimed in claim 25 wherein said first layer of nitride semiconductor overlays an entire width of said buffer structure, and said first metal layer overlays an entire width of said first layer of nitride semiconductor.

33. A structure as claimed in claim 25 wherein said first layer of nitride semiconductor overlays a portion of

said buffer structure, and said first metal layer overlays an entire width of said first layer of nitride semiconductor.

34. A method of making a semiconductor structure comprising the steps of:

(a) depositing aluminum directly on a surface of a silicon substrate to provide an aluminum-protected substrate; then

(b) depositing a nucleation layer of a nitride semiconductor on said aluminum-protected substrate; then

(c) epitaxially growing a buffer structure including one or more superlattices of nitride semiconductors on said nucleation layer; and then

(d) epitaxially growing an operative structure including one or more gallium nitride-based semiconductors on said buffer structure.

35. A method as claimed in claim 34 wherein said step of depositing said nucleation layer of said nitride semiconductor includes using  $\text{NH}_3$  as a reactant in contact with said aluminum-protected substrate.

36. A method as claimed in claim 35 wherein said step of depositing said nucleation layer includes metal organic chemical vapor deposition.

37. A method as claimed in claim 34 wherein said step of growing said buffer structure includes growing a first superlattice of nitride semiconductors directly on said nucleation layer.

38. A method as claimed in claim 34 wherein said step of epitaxially growing said operative structure includes growing a first layer of nitride semiconductor; said method further comprising depositing at least one first metal layer on said first layer of nitride semiconductor to form a Schottky contact therewith.

39. A method as claimed in claim 38 wherein said first layer of nitride semiconductor includes a gallium nitride-based semiconductor.

40. A method as claimed in claim 38 wherein said first layer of nitride semiconductor includes GaN.

41. A method as claimed in claim 38 further comprising depositing at least one further metal layer on another surface of said silicon substrate to form an ohmic contact therewith.

42. A method as claimed in claim 38 wherein said step of epitaxially growing said operative structure includes growing a further layer of nitride semiconductor atop said buffer structure prior to growing said first layer of nitride semiconductor such that said further layer of nitride semiconductor has a higher doping concentration than that of said first layer of nitride semiconductor.

43. A method as claimed in claim 42 wherein said further layer of nitride semiconductor includes a gallium nitride-based semiconductor.

44. A method as claimed in claim 42 wherein said further layer of nitride semiconductor includes GaN.

45. A method as claimed in claim 38 further comprising removing a portion of said first layer of nitride semiconductor such that said first layer of nitride semiconductor forms a mesa structure.

46. A method of making a semiconductor structure comprising the steps of:

(a) depositing a nucleation layer of a nitride semiconductor on a silicon substrate; then

(b) epitaxially growing a buffer structure including one or more superlattices of nitride semiconductors on said nucleation layer, said step of growing said buffer structure including growing a first superlattice of nitride semiconductors directly on said nucleation layer; and then

(c) epitaxially growing an operative structure including one or more gallium nitride-based semiconductors on said buffer structure.

47. A method as claimed in claim 46 wherein said step of growing said buffer structure includes growing an intermediate layer of a gallium-nitride semiconductor over said first superlattice and growing a second superlattice of nitride semiconductors over said intermediate layer.

48. A method as claimed in claim 46 wherein said step of epitaxially growing said operative structure includes growing a first layer of nitride semiconductor; said method further comprising depositing at least one first metal layer on said first layer of nitride semiconductor to form a Schottky contact therewith.

49. A method as claimed in claim 48 wherein said first layer of nitride semiconductor includes a gallium nitride-based semiconductor.

50. A method as claimed in claim 48 wherein said first layer of nitride semiconductor includes GaN.

51. A method as claimed in claim 48 further comprising depositing at least one further metal layer on another surface of said silicon substrate to form an ohmic contact therewith.

52. A method as claimed in claim 48 wherein said step of epitaxially growing said operative structure includes growing a further layer of nitride semiconductor atop said buffer structure prior to growing said first layer of nitride semiconductor such that said further layer of nitride semiconductor has a higher doping concentration than that of said first layer of nitride semiconductor.

53. A method as claimed in claim 51 wherein said further layer of nitride semiconductor includes a gallium nitride-based semiconductor.

54. A method as claimed in claim 51 wherein said further layer of nitride semiconductor includes GaN.

55. A method as claimed in claim 48 further comprising removing a portion of said first layer of nitride semiconductor such that said first layer of nitride semiconductor forms a mesa structure.

56. A method of making a semiconductor element comprising the steps of:

(a) epitaxially growing a nitride semiconductor structure on a silicon substrate; then

(b) bonding a carrier to said nitride semiconductor structure; then

(c) removing said silicon substrate from said nitride semiconductor structure.

57. A method as claimed in claim 56 further comprising the step of applying a base material other than silicon on said nitride semiconductor structure after removing said silicon substrate.

58. A method as claimed in claim 57 further comprising the step of removing said carrier after applying said base material.

59. A method as claimed in claim 58 further comprising the step of treating said nitride semiconductor structure before said step of bonding the carrier to form one or more devices in said structure.

60. A method as claimed in claim 58 further comprising the step of treating said nitride semiconductor structure to form one or more devices in said structure after said step of removing the carrier.

61. A method as claimed in claim 58 wherein said step of applying a base material includes depositing said base material on said nitride semiconductor structure to form a film of said base material on a bottom surface of the nitride semiconductor structure, remote from said carrier.

62. A method as claimed in claim 61 wherein said step of depositing said base material includes depositing a base

material selected from the group consisting of aluminum nitride and diamond.

63. A semiconductor element including a nitride semiconductor structure having one or more epitaxially-grown layers and a base supporting said nitride semiconductor structure, said base being a structure other than a substrate used in epitaxial growth of said nitride semiconductor structure, the element not including the substrate used in epitaxial growth of said nitride semiconductor structure.

64. A semiconductor element as claimed in claim 63 wherein said base is formed from a material selected from the group consisting of nitride semiconductors and diamond.

65. A method of making a semiconductor structure on a silicon substrate comprising the steps of:

(a) depositing a layer of aluminum less than about 10 atomic monolayers thick on the top surface of the substrate to form an aluminum-protected substrate; and then

(b) depositing at least one nitride semiconductor on the aluminum-protected substrate.

66. A method as claimed in claim 65 wherein said step of depositing a nitride semiconductor includes exposing the aluminum-protected substrate to an atmosphere which includes one or more organometallic compounds and ammonia.

67. A semiconductor structure made by a process as claimed in claim 65.

68. A vertical current conduction Schottky diode comprising:

a silicon substrate;

at least one layer of nitride semiconductor overlying a surface of said silicon substrate;

at least one first metal layer overlying said layer of nitride semiconductor and forming a Schottky contact therewith; and

at least one further metal layer overlying another surface of said silicon substrate and forming an ohmic contact therewith.

69. A structure as claimed in claim 68 wherein said at least one layer of nitride semiconductor includes a gallium nitride-based semiconductor.

70. A Schottky diode as claimed in claim 68 wherein said at least one layer of nitride semiconductor includes GaN.

71. A Schottky diode as claimed in claim 68 further comprising a buffer structure disposed between said silicon substrate and said layer of nitride semiconductor.

72. A Schottky diode as claimed in claim 71 wherein said buffer structure includes at least one superlattice disposed between said silicon substrate and said layer of nitride semiconductor that includes a plurality of nitride semiconductors of different compositions.

73. A Schottky diode as claimed in claim 71 wherein said buffer structure includes a first superlattice, an intermediate layer of nitride semiconductor overlying said first superlattice, and a second superlattice overlying said intermediate layer.

74. A Schottky diode as claimed in claim 68 further comprising a layer of aluminum that directly overlays said silicon substrate.

75. A Schottky diode as claimed in claim 74 further comprising a polycrystalline nucleation layer that includes a nitride semiconductor and which directly overlays said aluminum layer.

76. A Schottky diode as claimed in claim 68 further comprising a further layer of nitride semiconductor disposed between said silicon substrate and said first layer of nitride semiconductor; said further layer of nitride semiconductor having a higher doping concentration than that of said first layer of nitride semiconductor.

77. A Schottky diode as claimed in claim 76 wherein said further layer of nitride semiconductor includes a gallium nitride-based semiconductor.

78. A Schottky diode structure as claimed in claim 76 wherein said further layer of nitride semiconductor includes GaN.

79. A Schottky diode as claimed in claim 68 wherein said layer of nitride semiconductor overlays an entire width of said silicon substrate, and said first metal layer overlays an entire width of said first layer of nitride semiconductor.

80. A Schottky diode as claimed in claim 68 wherein said layer of nitride semiconductor overlays a portion of said silicon substrate, and said first metal layer overlays an entire width of said layer of nitride semiconductor.

81. A method of making a vertical current conduction Schottky diode comprising:

forming at least one layer of nitride semiconductor on a surface of a silicon substrate;

depositing at least one first metal layer on said layer of nitride semiconductor to form a Schottky contact therewith; and

depositing at least one further metal layer on another surface of said silicon substrate to form an ohmic contact therewith.

82. A method as claimed in claim 81 wherein said one layer of nitride semiconductor includes a gallium nitride-based semiconductor.

83. A method as claimed in claim 81 wherein said one layer of nitride semiconductor includes GaN.

84. A method as claimed in claim 81 further comprising forming a buffer structure on said surface of said silicon substrate prior to forming said layer of nitride semiconductor.

85. A method as claimed in claim 84 wherein said step of forming said buffer structure includes growing at least one superlattice that includes a plurality of nitride semiconductors of different compositions.

86. A method as claimed in claim 84 wherein said step of forming said buffer structure includes growing a first superlattice, growing an intermediate layer of nitride semiconductor overlying said first superlattice, and growing a second superlattice overlying said intermediate layer.

87. A method as claimed in claim 81 further comprising depositing a layer of aluminum directly on said silicon substrate.

88. A method as claimed in claim 87 further comprising forming a polycrystalline nucleation layer that includes a nitride semiconductor directly on said aluminum layer.

89. A method as claimed in claim 81 further comprising forming a further layer of nitride semiconductor prior to forming said first layer of nitride semiconductor; said further layer of nitride semiconductor having a higher doping concentration than that of said first layer of nitride semiconductor.

90. A method as claimed in claim 89 wherein said further layer of nitride semiconductor includes a gallium nitride-based semiconductor.

91. A method as claimed in claim 89 wherein said further layer of nitride semiconductor includes GaN.

92. A method as claimed in claim 81 further comprising removing a portion of said layer of gallium nitride such that said layer of gallium nitride forms a mesa structure.